Fig. 1

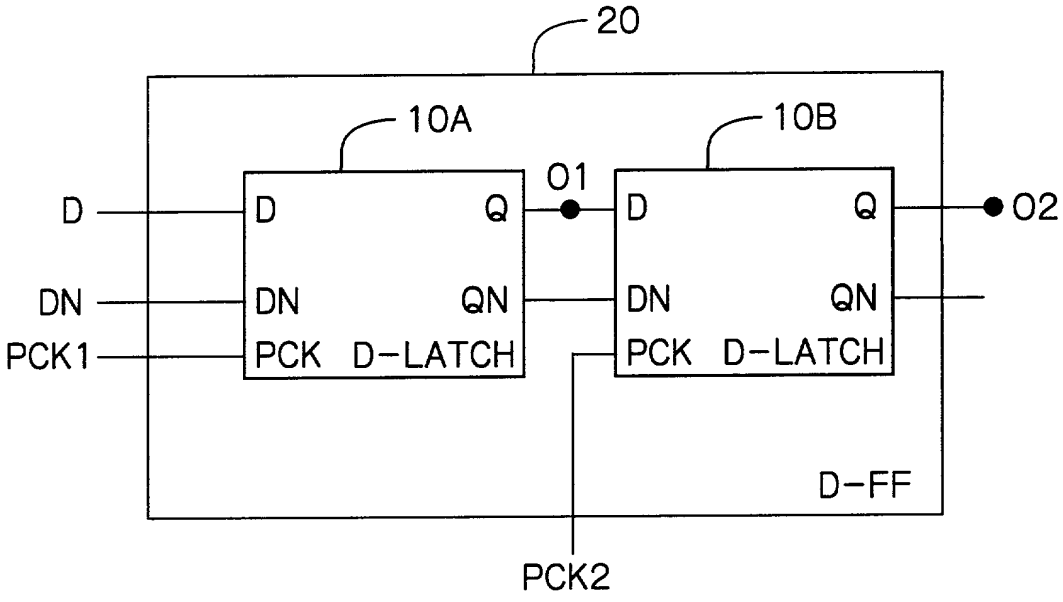

20
10A
10B
D
DN
PCK1
D
Q
DN
QN
PCK D-LATCH
O1
D
Q
DN
QN
PCK D-LATCH
O2
D-FF
PCK2

Fig. 2A

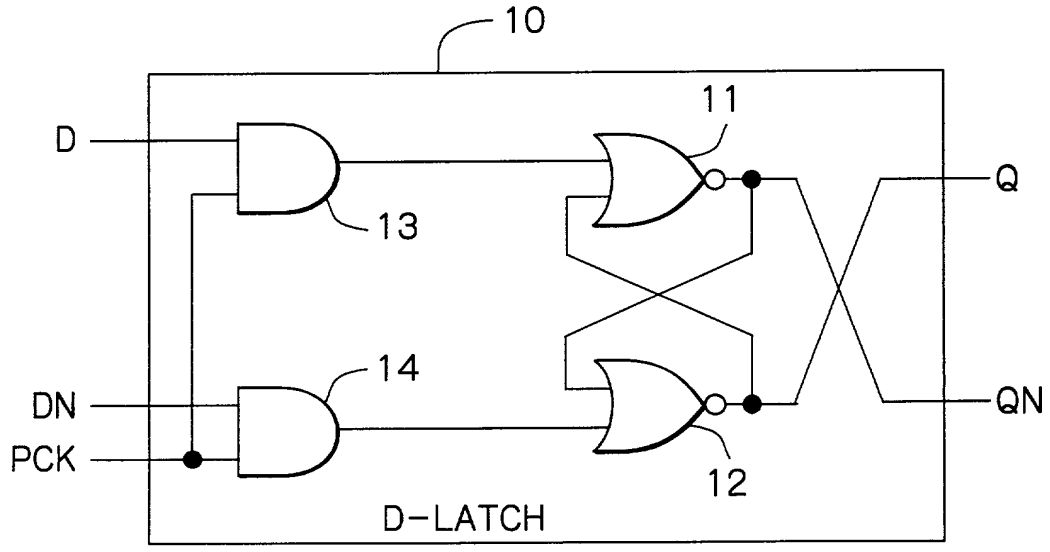

10
D
DN
PCK
13
14
11
12
Q
QN
D-LATCH

Fig. 2B

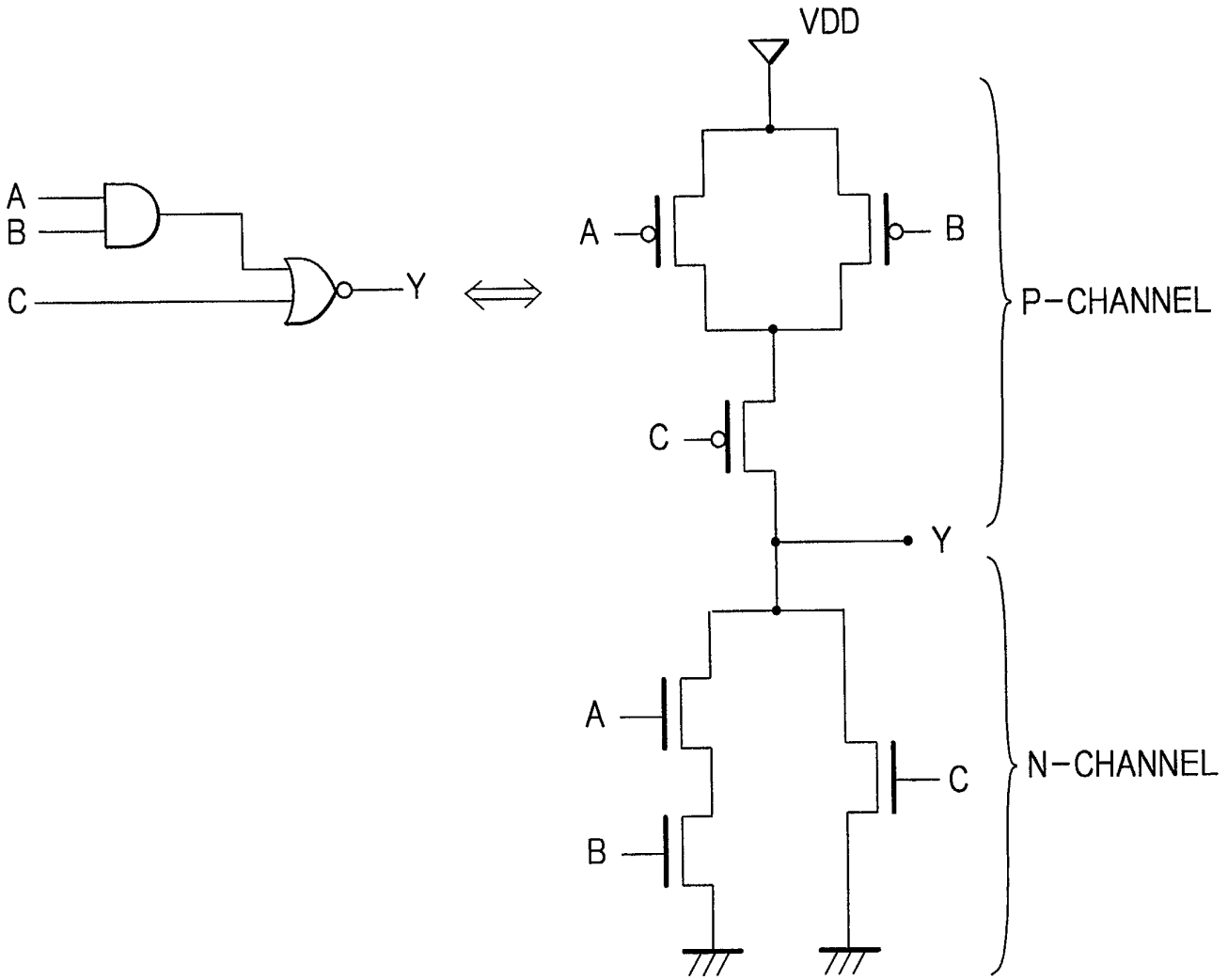


Fig. 2C

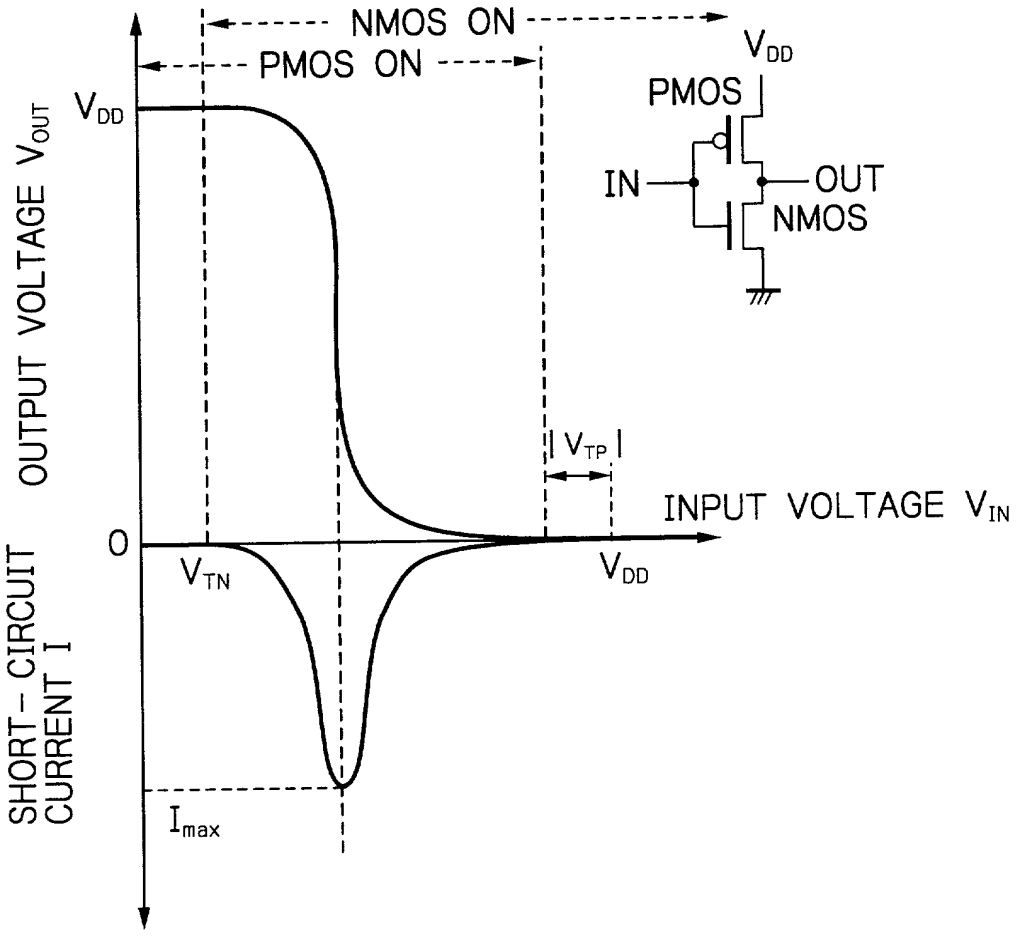

NMOS ON
PMOS ON
V_{DD}
PMOS
IN
OUT
NMOS
OUTPUT VOLTAGE V_{OUT}
V_{DD}
$|V_{TP}|$
INPUT VOLTAGE V_{IN}
0
V_{TN}
V_{DD}
SHORT-CIRCUIT CURRENT I
I_{max}

Fig. 3

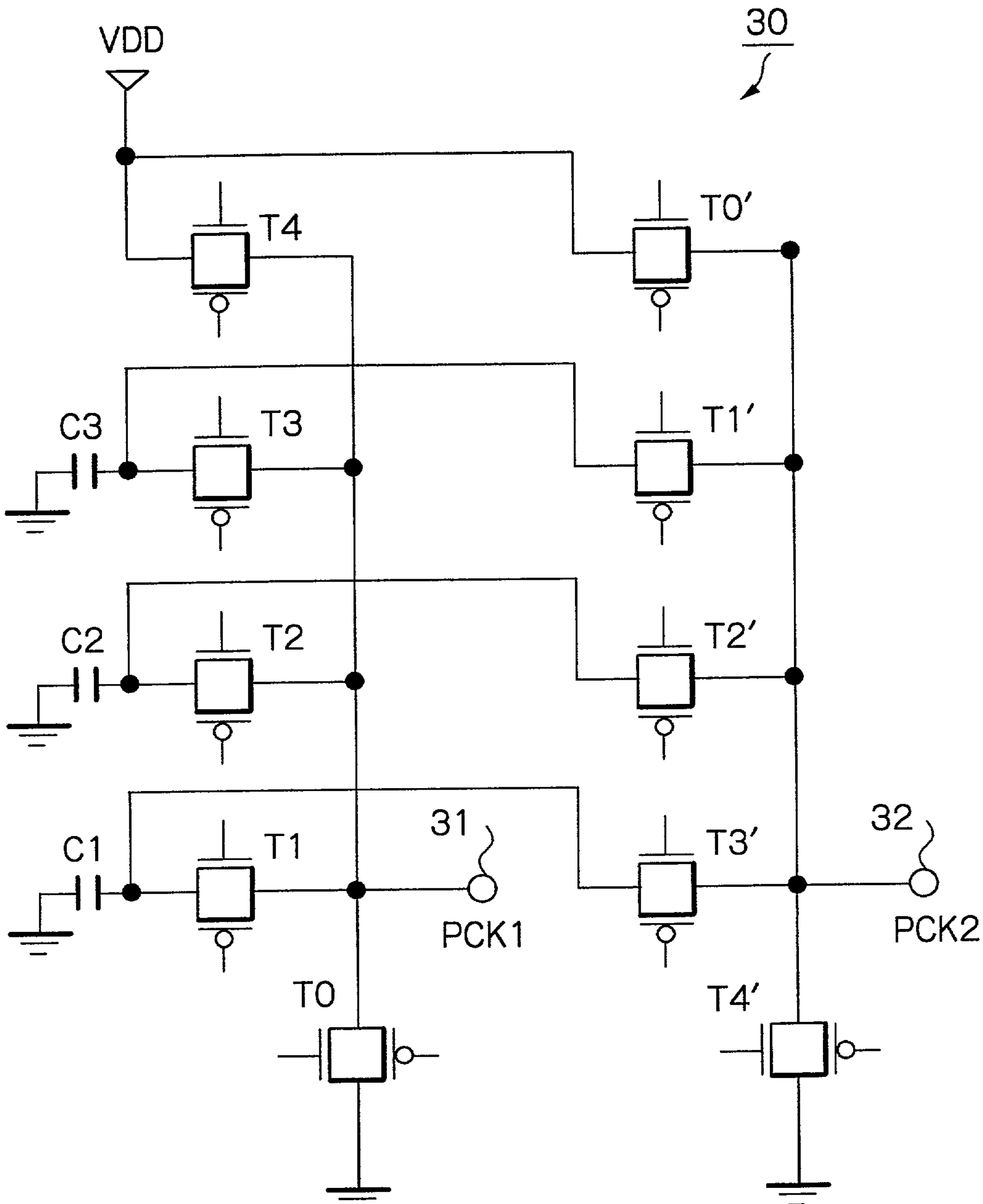


Fig. 4

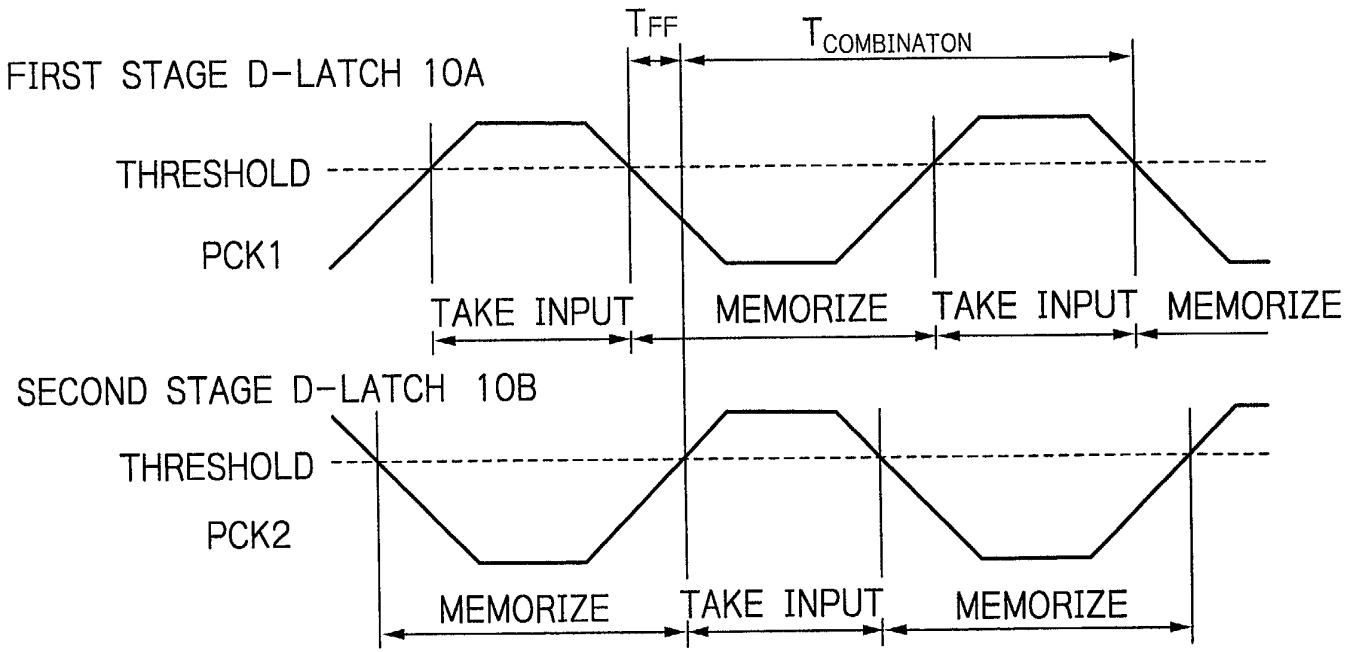

TFF
TCOMBINATON
FIRST STAGE D-LATCH 10A
THRESHOLD
PCK1
TAKE INPUT
MEMORIZE
TAKE INPUT
MEMORIZE
SECOND STAGE D-LATCH 10B
THRESHOLD
PCK2
MEMORIZE
TAKE INPUT
MEMORIZE

Fig. 5

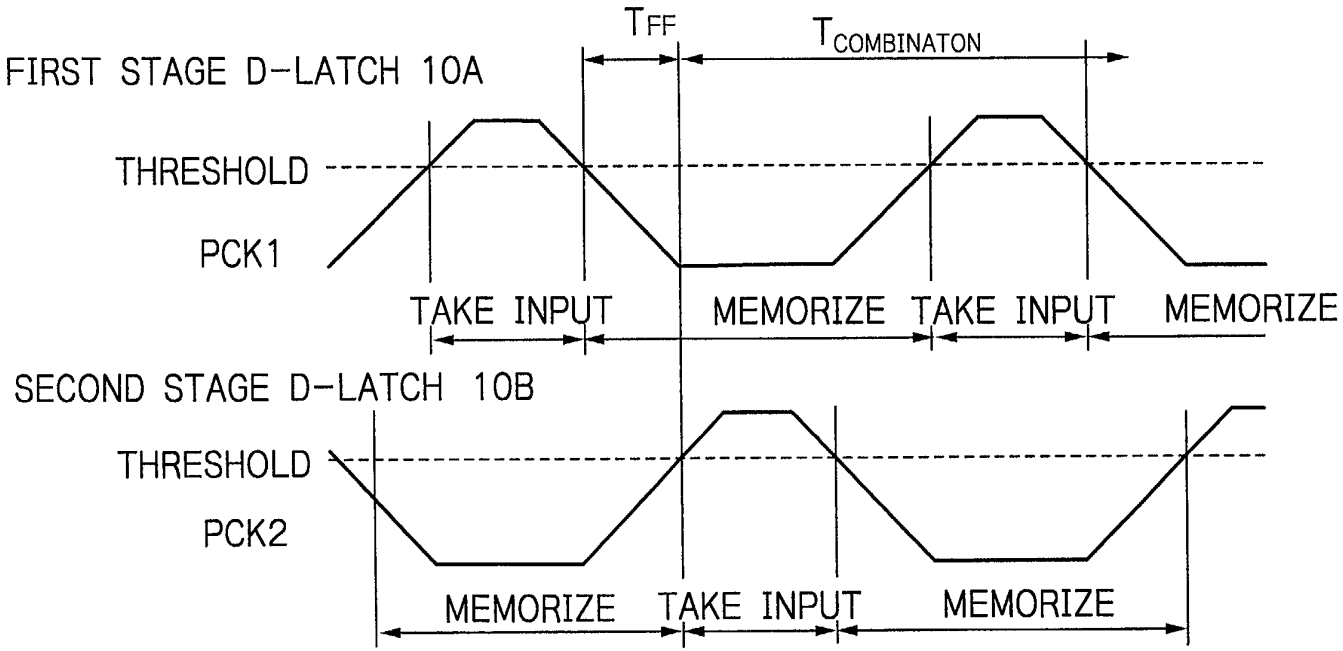

TFF
TCOMBINATON
FIRST STAGE D-LATCH 10A
THRESHOLD
PCK1
TAKE INPUT
MEMORIZE
TAKE INPUT
MEMORIZE
SECOND STAGE D-LATCH 10B
THRESHOLD
PCK2
MEMORIZE
TAKE INPUT
MEMORIZE

Fig. 6

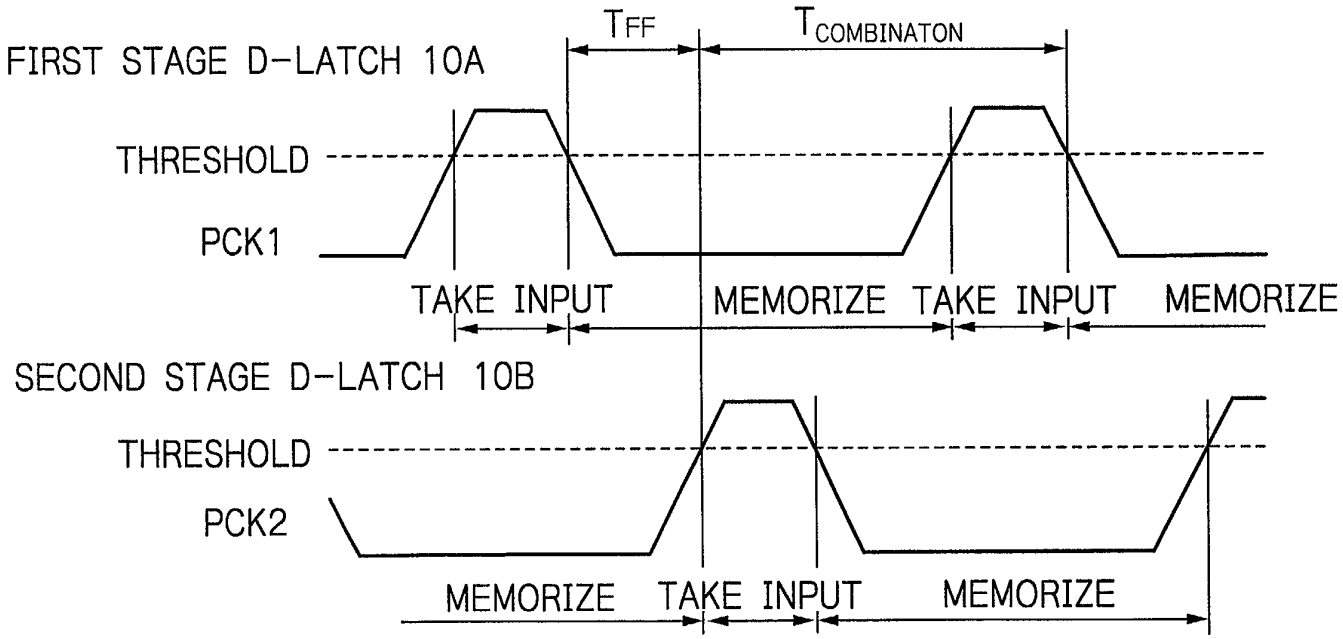

FIRST STAGE D-LATCH 10A
THRESHOLD
PCK1
TFF
TCOMBINATON
TAKE INPUT
MEMORIZE
TAKE INPUT
MEMORIZE
SECOND STAGE D-LATCH 10B
THRESHOLD
PCK2
MEMORIZE
TAKE INPUT
MEMORIZE

Fig. 7

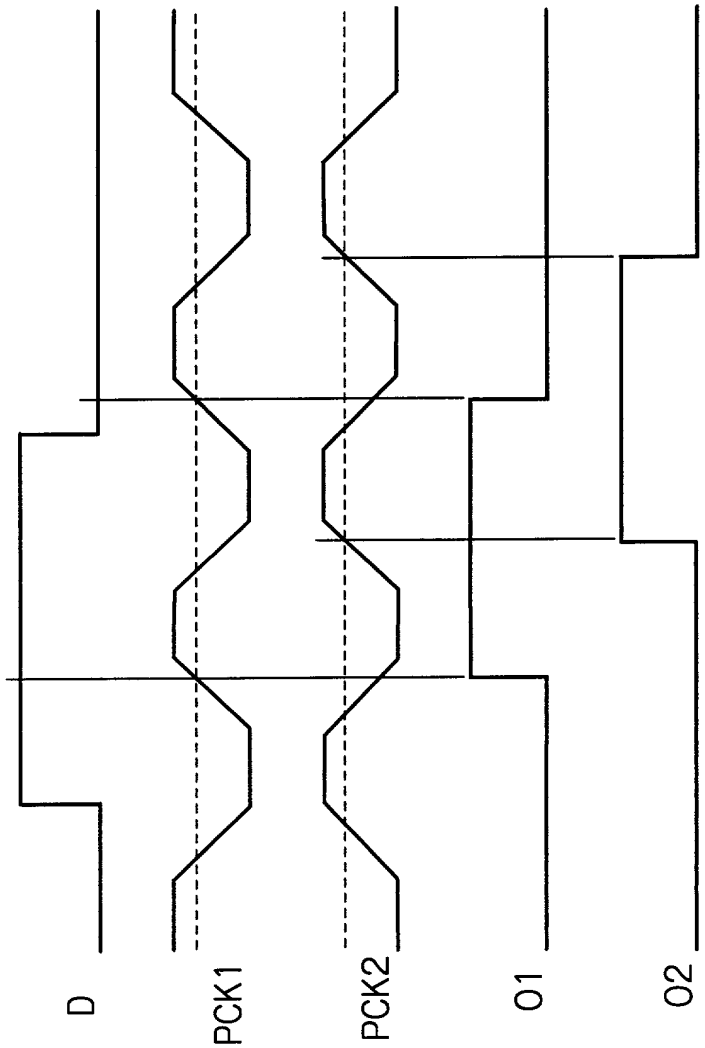


Fig. 8

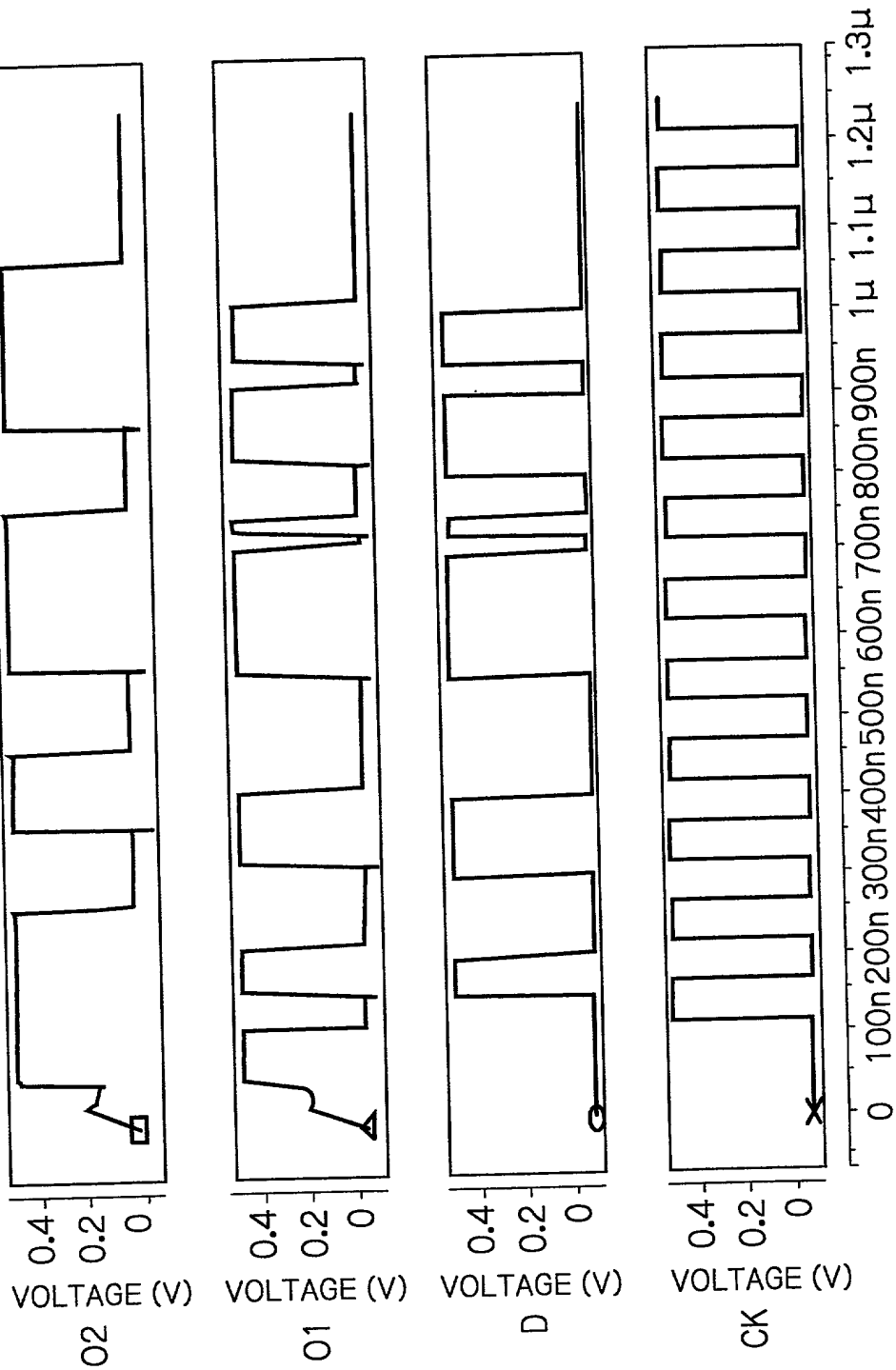
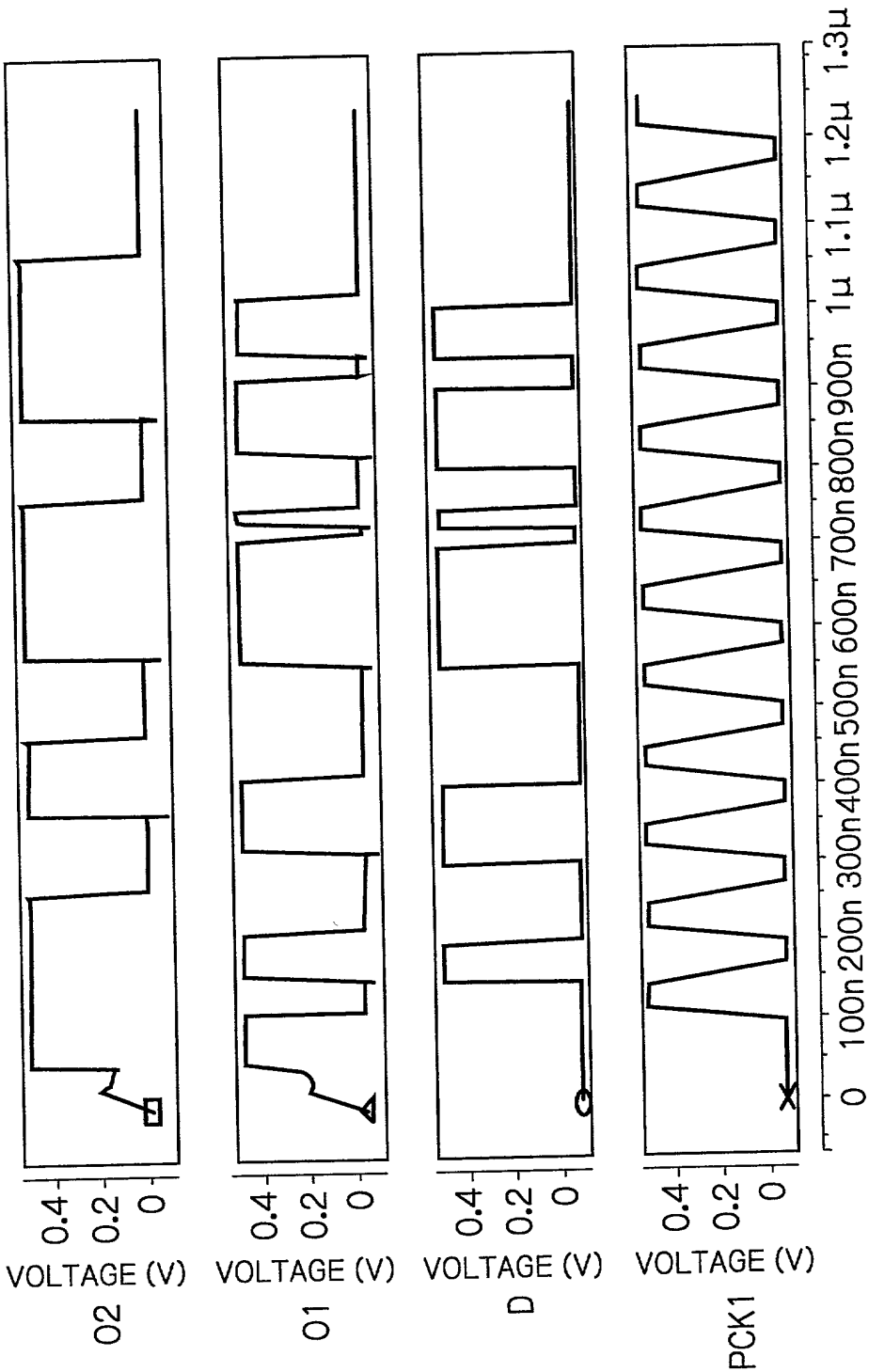

O2
O1
D
CK
VOLTAGE (V)
0.4
0.2
0
0 100n 200n 300n 400n 500n 600n 700n 800n 900n 1µ 1.1µ 1.2µ 1.3µ
TIME (sec)

Fig. 9



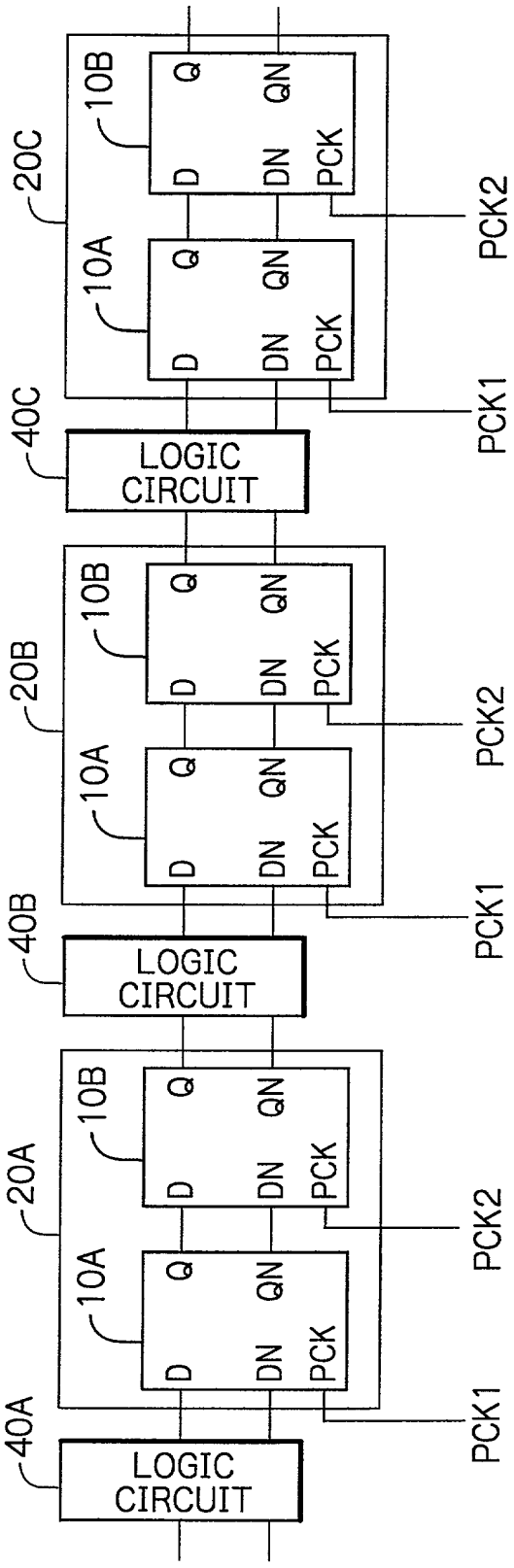

20C
10B
10A
40C
LOGIC CIRCUIT
20B
10B
10A
40B
LOGIC CIRCUIT
20A
10B
10A
40A
LOGIC CIRCUIT
Q
QN
D
DN
PCK
PCK2
PCK1

Fig. 10

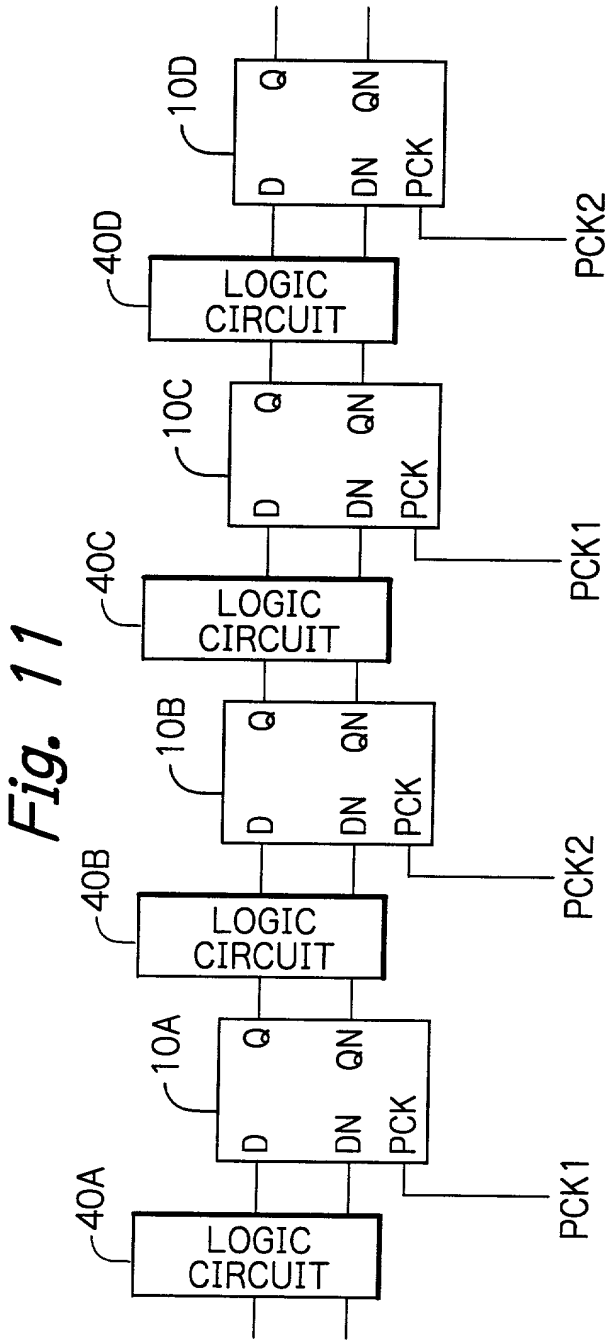

10D
Q
QN
D
DN
PCK
PCK2
40D
LOGIC CIRCUIT
10C
Q
QN
D
DN
PCK
PCK1
40C
LOGIC CIRCUIT
10B
Q
QN
D
DN
PCK
PCK2
40B
LOGIC CIRCUIT
10A
Q
QN
D
DN
PCK
PCK1
40A
LOGIC CIRCUIT

Fig. 11

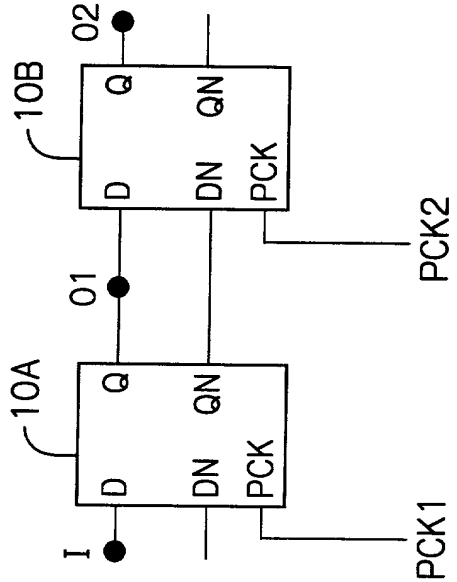

02
10B
Q
QN
D
DN
PCK
PCK2
01
10A
Q
QN
D
DN
PCK
PCK1
I

Fig. 12

Fig. 13

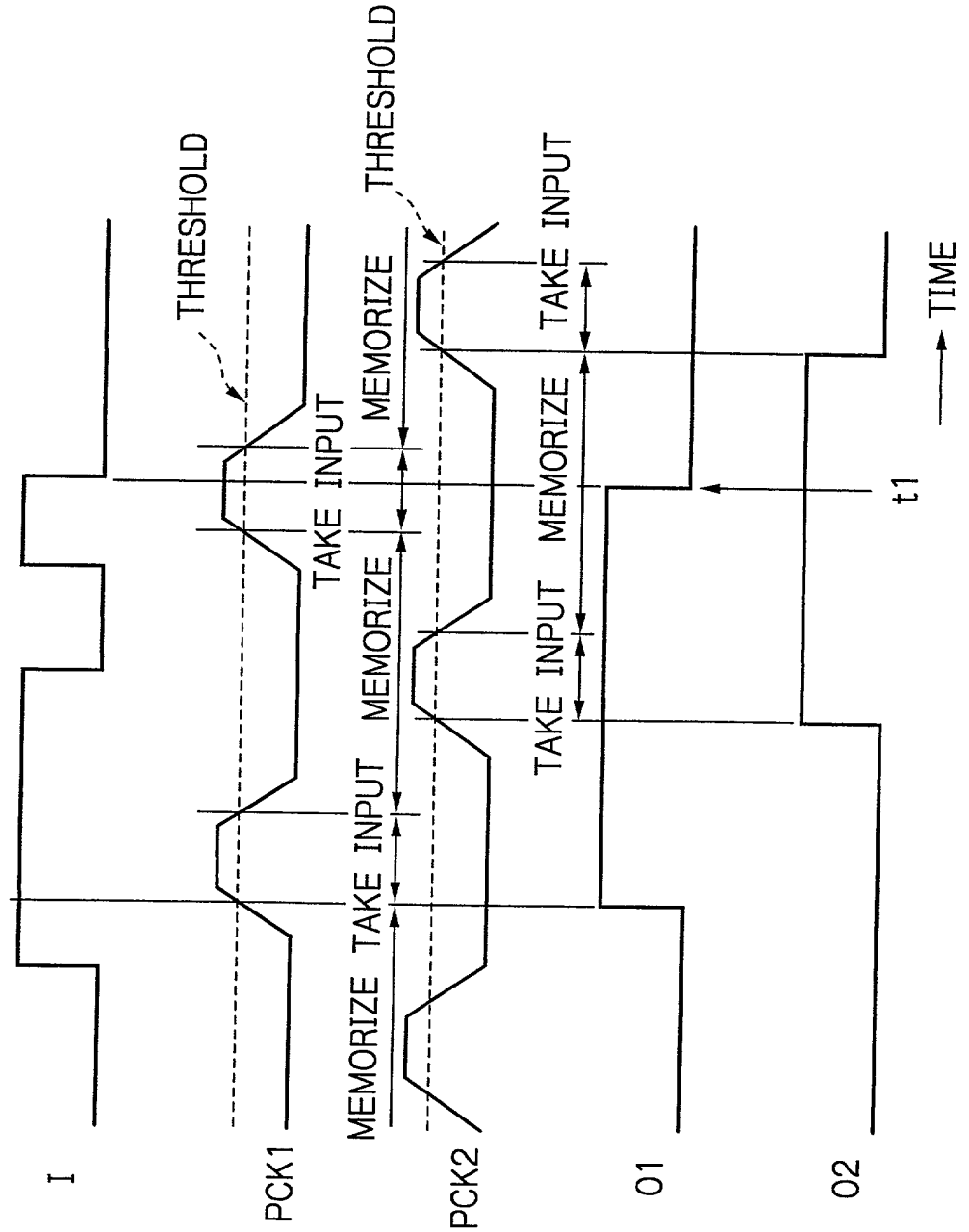

I
PCK1
PCK2
O1
O2
THRESHOLD
THRESHOLD
TAKE INPUT
MEMORIZE
MEMORIZE
TAKE INPUT
TAKE INPUT
MEMORIZE
MEMORIZE
TAKE INPUT
t1
TIME

Fig. 14

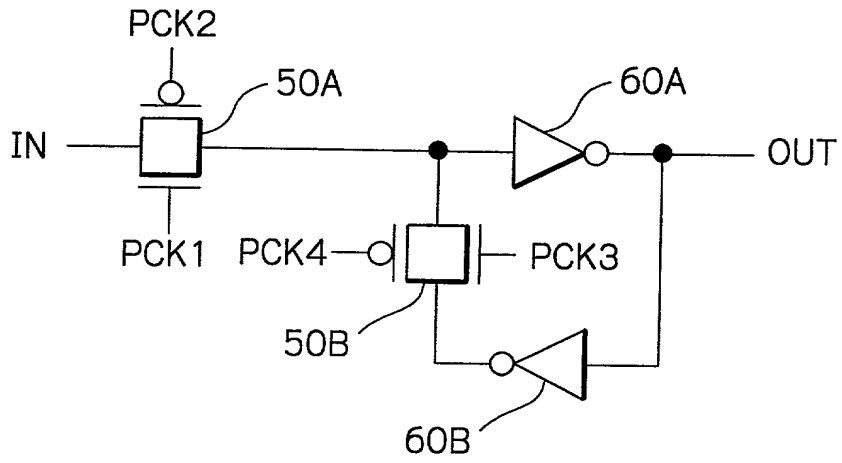


Fig. 15

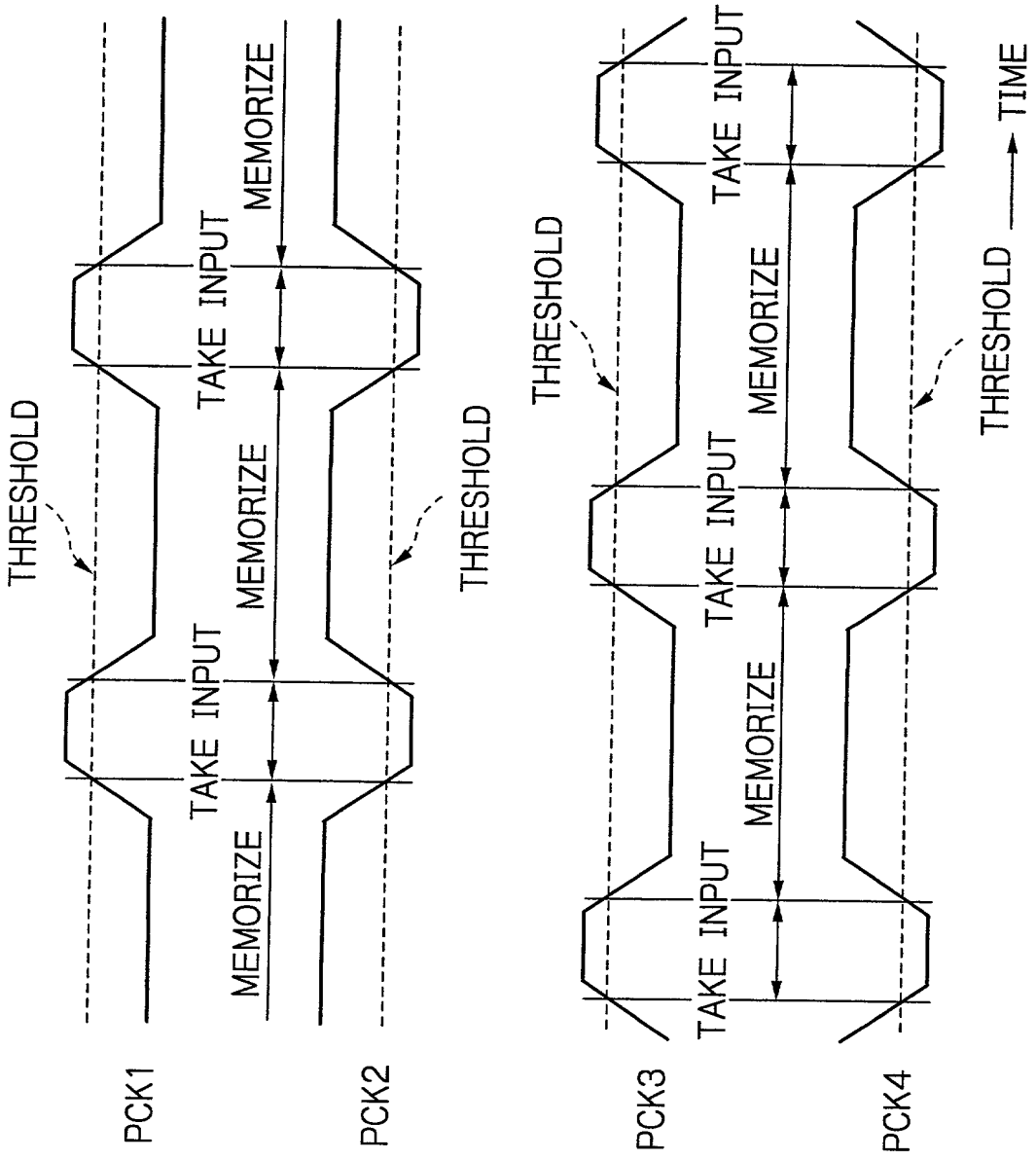

THRESHOLD
TAKE INPUT
MEMORIZE
MEMORIZE
TAKE INPUT
PCK1
PCK2
THRESHOLD
THRESHOLD
TAKE INPUT
MEMORIZE
TAKE INPUT
MEMORIZE
PCK3
PCK4
THRESHOLD
TIME

Fig. 16

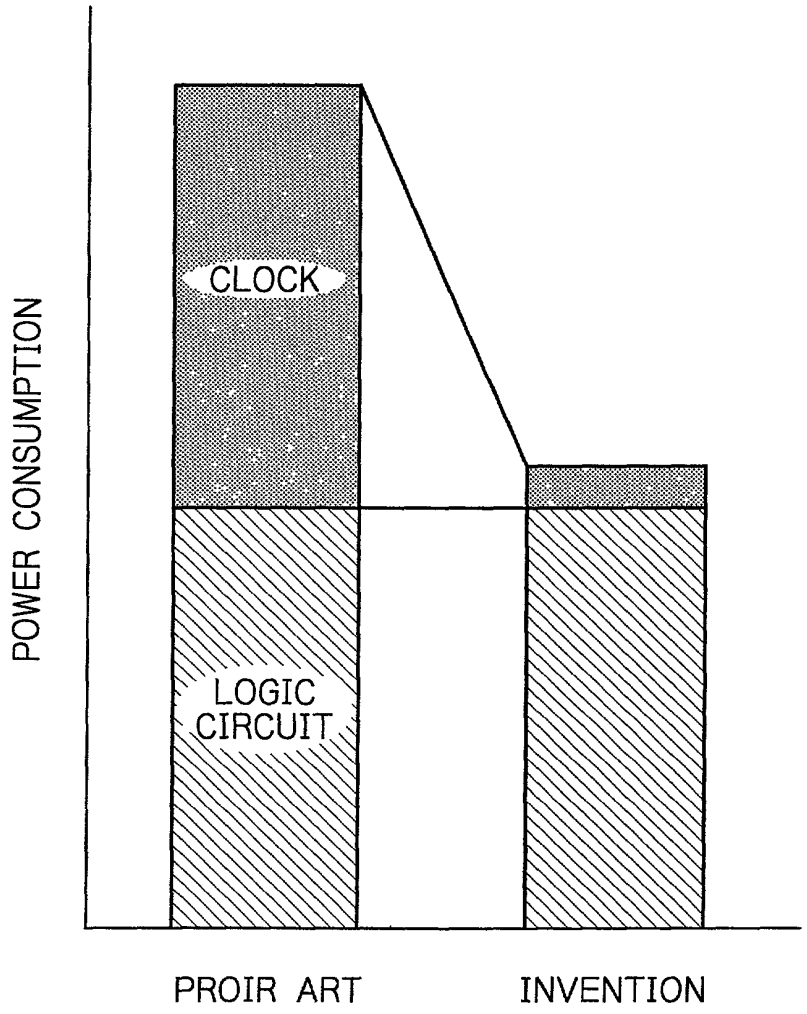

POWER CONSUMPTION
CLOCK
LOGIC CIRCUIT
PROIR ART
INVENTION

Fig. 17 PRIOR ART

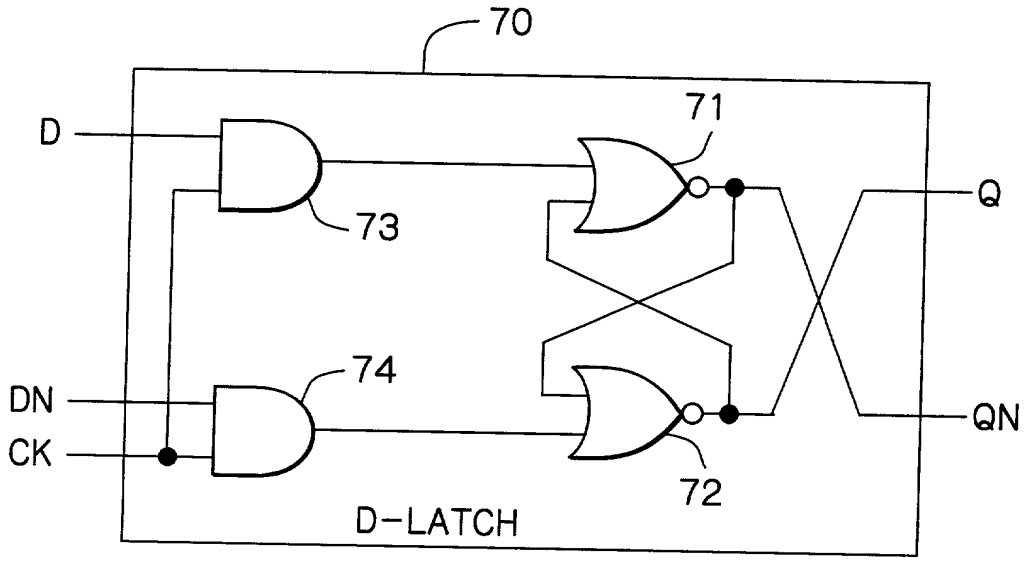


Fig. 18 PRIOR ART

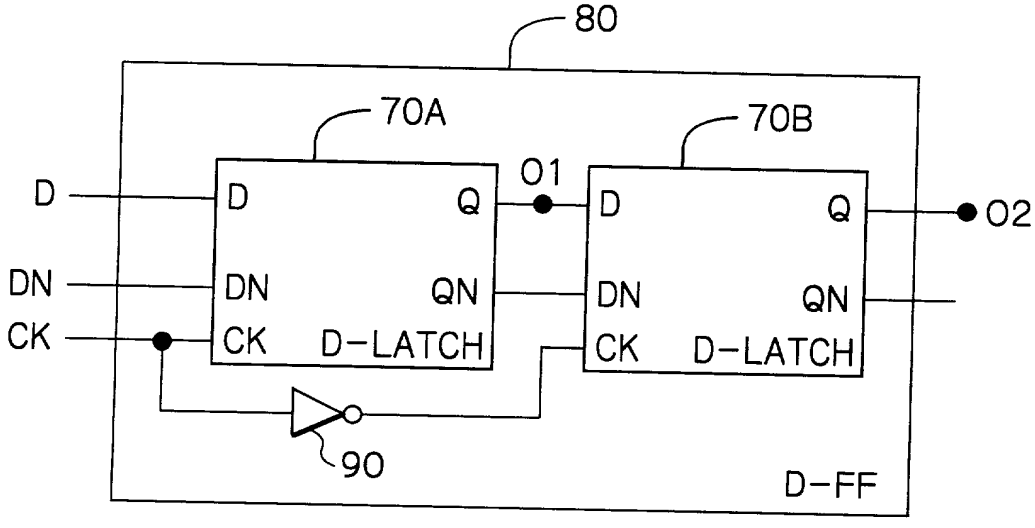


Fig. 19 PRIOR ART